

Libraries

Name	Process	Form Factor
RGO_GF40_25V5_LP_20C	LP	Staggered CUP
RGO_GF40_25V5_LP_40C	LP	Inline CUP

Summary

The 5V GPIO library provides general purpose bidirectional I/O cells. These programmable, multi-voltage I/O's give the system designer the flexibility to design to a wide range of performance targets.

Additionally, this library provides a full complement of cells to support the assembly of a functional pad ring by abutment for GPIO and other I/O library offerings from Aragio Solutions that use a compatible pad ring bus structure.

This 40nm library is available in both staggered CUP and inline CUP wire bond implementations with a staggered flip chip option.

The included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
 - 2kV ESD Human Body Model (HBM)
 - 200V ESD Machine Model (MM)
 - 500V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

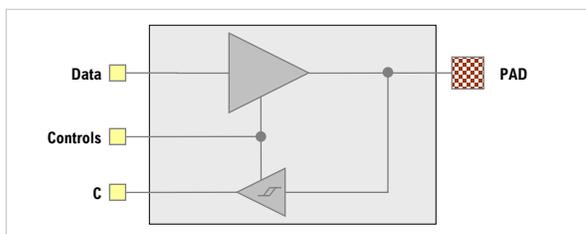
Cell Size & Form Factor

- Staggered (pad-limited) – $35\mu\text{m} \times 200\mu\text{m}$
- Inline (core-limited) – $50\mu\text{m} \times 140\mu\text{m}$

Recommended operating conditions

Description	Min	Nom	Max	Units
V_{VDD} Core supply voltage	0.90	1.0	1.10	V
V_{DVDD} I/O supply voltage	0.99	1.1	1.21	V
T_{J} Junction temperature	-40	25	175	$^\circ\text{C}$
V_{PAD} Voltage at PAD	$V_{\text{DVSS}} - 0.3$	-	$V_{\text{DVDD}} + 0.3$	V

SRx_BI_SDS_5V_STB



Bidirectional GPIO Driver Features

- 5V operation
- LVCMOS / LVTTTL input with selectable hysteresis
- Programmable drive strength (rated 2mA to 12mA)
- Selectable output slew rate
- Optimized for EMC with SSO factor of 8
- Open-drain output mode
- Programmable input options (hi-Z/pull-up/pull-down/repeater)
- Power sequencing independent design with Power-On Control

In full-drive mode, this driver can operate to frequencies in excess of 100MHz with 15pF external load and 125 MHz with 10pF load. Actual frequency limits are load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

Support Cells

Name	Description
Digital Pads	
STx_IN_001_5V_NC	Input-only buffer
I/O Power / Ground Pads	
PWx_VD_RDO_5V	I/O power (DVDD)
PWx_VS_RDO_5V	I/O ground (DVSS)
Core Power / Ground Pads	
PWx_VD_RCD_1250V	Core power (VDD)
PWx_VS_RCD_1250V	Core ground (VSS)
Analog Pads	
ANx_BI_DWR_5V	Isolated analog input cell
Analog Power / Ground Pads	
PWx_VD_ANA_1250V	Analog power (AVDD) 1.0V
PWx_VS_ANA_1250V	Analog ground (AVSS)
PWx_VD_ANA_5V	Analog power (ADVDD) 3.3V
PWx_VS_ANA_5V	Analog ground (ADVSS)
Support Pads	
SPx_CO_000_5V	Corner cell (rail splitter)
SPx_CO_001_5V	Corner cell (continuous)
SPx_SP_000_5V	0.1 μm spacer
SPx_SP_001_5V	1 μm spacer
SPx_SP_005_5V	5 μm spacer
SPx_SP_010_5V	10 μm spacer
SPx_RS_005_5V	Rail splitter
SPP_RE_SVR_5V	VREF generator
SPP_SP_POC_5V	POC generator

Characterization Corners

Nominal VDD	Model	VDD	DVDD = 5V	Temperature
1.2	FF	+5%	+10%	-40°C
	FFF	+5%	+10%	125°C
	FFF	+5%	+10%	150°C
	FFF	+5%	+10%	175°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
	SS	-10%	-10%	150°C
	SS	-10%	-10%	175°C
	1.1 / 1.0	FF	+10%	+10%
FFF		+10%	+10%	125°C
FFF		+10%	+10%	150°C
FFF		+10%	+10%	175°C
TT		nominal	nominal	25°C
SS		-10%	-10%	-40°C
SS		-10%	-10%	125°C
SS		-10%	-10%	150°C

CUP Cells

Staggered CUP Cells	
CUP_GF40NM_5V_79P9X43P6_IN	79.9µm X 43.6µm Inner
CUP_GF40NM_5V_79P9X43P6_OUT	79.9µm X 43.6µm Outer
CUP_GF40NM_5V_79P9X44P6_IN	79.9µm X 44.6µm Inner
CUP_GF40NM_5V_79P9X44P6_OUT	79.9µm X 44.6µm Outer
CUP_GF40NM_5V_FC	Flip chip structure
Inline CUP Cells	
CUP_GF40NM_5V_85X43_INLINE	85µm X 43µm Inline

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